ABSTRACT OF THE DISCLOSURE

A bridge circuit includes two FIFO circuits each having an associated FIFO control circuit. In each FIFO control circuit, a write pointer register and a read pointer register for controlling the storage location for writing to and reading from the FIFO circuit are each controlled by control logic. The control logic is responsive to comparators which receive and compare the write pointer value and the retimed read pointer value to control the write pointer register, and receive and compare the read pointer value and the retimed write pointer value to control the read pointer register. The retiming circuits are configurable in response to a mode signal to provide different degrees of retiming. The maximum number of storage locations that can be full at any one time is a fixed limit.